Amendments to the Specification:

Please replace paragraph [0013], [0016], [0017], [0021], and [0036] with the following amended paragraphs:

[0013] Figure 1 is a diagram illustrating a system 100 in which one embodiment of the invention can be practiced. The system 100 includes N processors 110_1 to 110_N, N master buses 115_1 to 115_N, a master bus interface circuit 120, K slave buses 135_1 to 135_K, slave devices 140_{jk} (j=1, . . .,K, k = 1,...,L, 1,. . .,M, 1,. . ., P[[K]]), a common memory interface 150, and a common memory 160.

[0016] The K slave buses 135_1 to 135_K provide access to slave devices. Each of the K slave buses 135_1 to 135_K is connected to a number of slave devices 140_{jk} (j=1, . . .,K, k = 1,...,L, 1,. . .,M, 1,. . ., P[[K]]),. The L slave devices 140_{11} to 140_{1L} are connected to the slave bus 135_1, . . ., the M slave devices 140_{21} to 140_{2M} are connected to the slave bus 135_2, . . ., the P slave devices 140_{K1} to 140_{KP} are connected to the slave bus 135_K. The K slave buses 135_1 to 135_K may be homogeneous or heterogeneous, i.e., there may be a set of slave buses of the same type and other sets of slave buses of different types, or all the slave buses are of the same type. The slave devices may be any type of device that cannot or does not have control of the master buses. Examples of these slave devices 140_{jk} (j=1, . . .,K, k = 1,...,L, 1,. . .,M, 1,. . ., P[[K]]) include slave processors, micro-controllers, memory devices, peripheral input/output (I/O) devices, network interface, printer controller, disk drive controller, media interface (e.g., graphics, audio, video), etc. Memory devices include random access memory (RAM), read only memory (ROM), flash memory, or even mass storage device such as compact disk (CD) ROM, floppy diskette, and hard drive.

[0017] The common memory interface 150 is connected to the K slave buses 135_1 to 135_K and the common memory 160 to allow any of the N processors 110_1 to 110_N, or even any of the slave devices 140_{jk} (j=1, . . .,K, k = 1,...,L, 1,. . .,M, 1,. . ., P[[K]]) to access the common memory 160. The common memory 160 is a memory that is common to all the N processors 110_1 to 110_N. In other words, any of the N processors 110_1 to 110_N can access the common memory 160 via an appropriate data path. Typically, the common memory 160 stores information that is relevant to most or all processors and slave devices. The common memory

160 may contain data, records, structures, linked lists, configuration data, status information, messages, mails, etc. The common memory 160 may also contain program segments, routines, functions, library of functions, etc., that can be used by any of the N processors 110_1 to 110_N. The common memory 160, therefore, may be program memory, data memory, or a combination of both.

[0021] The processor 110_N follows a data path 230. For example, the processor 110_N is a microprocessor fetching instructions from a program memory stored in slave device 140_{K1}. The data path 230 goes through the master bus 115_N, the bus controller $\underline{130_N}$ ~~135_N~~, the slave bus 135_K ~~$135K$~~, to the slave device 140_{K1}. The processor 110_N may also follow data path 240 to go through the common memory interface 150 and to the common memory 160.

[0036] The multiplexer 410 ~~420~~ has K inputs connected to K slave buses 135_1 to 135_K. The output of the multiplexer 410 ~~420~~ is connected to the common memory 160. The multiplexer 410 ~~420~~ transfers the common memory access information to the common memory 160 using a select signal provided by the interface controller 430. The common memory access information includes memory select signals and data to be written into the common memory 160.